REMARKS

All claims were rejected as being anticipated by Chong, *et al.* (6,311,212) or as being unpatentable over Chong, *et al.* in view of Barkey (5,825,748), Stephens, *et al.* (6,345,040) and/or Thorson, *et al.* (5,701,406). The rejections are respectfully traversed and reconsideration is requested.

The present invention was developed for a system in which information units are assigned to virtual channels within a router. For example, each virtual channel may be associated with a destination port of the overall fabric. Data received at any port is stored in a buffer associated with the port and a particular virtual channel. Data stored in the virtual channel buffers may be read from the buffers in an arbitrary order dependent on availability of downstream buffer space for each virtual channel. In the prior system disclosed in WO99/11033 (cited in the background of the present invention and corresponding to U.S. Patent 6,370,145) an individual buffer space was provided for each virtual channel at each port in each router. With a very large number of virtual channels, that approach is not feasible.

The present invention is based on the recognition that, although data must be independently stored in the many virtual channels and freely readable from any virtual channel buffer so that one stalled channel does not block another, most virtual channel buffers are at any time empty. Thus, in accordance with the present invention, the buffer space is shared by multiple virtual channels. For example, in the approach of Figure 7, a pointer array 300 includes pointer information for each virtual channel. Where data is stored in a virtual channel, the virtual channel pointers may point to on-chip buffers 400 which are selected from the buffers that are available. Thus, buffer 3 may at one time store data for virtual channel 4, but after that buffer is free, may be assigned to another virtual channel. In accordance with a further aspect of the invention, where the on-chip storage 400 becomes full, selected data may be stored in off-chip memory 200. In the alternative embodiments of Figures 8 and 9, the on-chip memory serves as a set associative cache through which virtual channels share on-chip buffer space.

The on-chip cache memory of Chong, *et al.* is not related to buffer storage of information units, eg. packets or flits, which are received by a router at its input link. Rather, the cache memory of Chong, *et al.* is for storage of static reference information which is otherwise stored off-chip. A virtual circuit descriptor identifier from a packet is used to index the cache memory

and local memory to extract descriptors such as packet type, packet size and protocols (column 1, lines 39-40, column 2, lines 1-17). Thus, it is not the information units received in a packet which are stored in the cache and local memory, but static information which remains for reference within the network processor.

By contrast, the present invention relates to handling of the massive amounts of information units, that is, the data of the packets or the like. In certain embodiments, much, or even all, of the off-chip buffer storage may remain empty if the on-chip buffer space is able to handle the bandwidth. Only with higher system loads is overflow required to be transferred to the off-chip space.

Nowhere does Chong, *et al.* suggest handling of the information units received at an input link in a cache-like process. The undersigned has only noted reference to such information at column 4, lines 50-54 where it is noted that the receiver engine "passes the cell payload to either an internal cell buffer, internal memory 80 or local memory 115." There is no suggestion that the system would store the cell payload both internally in a cache and off-chip.

The independent claims have been amended to highlight that the rapidly accessible buffers of the present invention store received information units as opposed to reference information. The cache of Chong, *et al.* does not include "buffers which store information units received at an input link." Nor do any of the other cited references teach the two sets of buffers for information units as claimed in the independent claims.

Further, the references do not suggest many of the features of the dependent claims.

For example, with respect to claims 5-7, 20-22, 35 and 43, Chong, *et al.* does not teach a set associative cache. Rather, the CAM of Chong, *et al.* allows every entry of the cache to be searched in a fully associative cache.

Claims 11, 12, 26 and 27 relate to the handling of information units being transferred from the first set of buffers to the second set of buffers. No such features are provided in Chong, *et al.* since, with a miss, Chong, *et al.* does not need to transfer data off-chip. The data is already statically stored off-chip.

With respect to method claim 16, it is similarly noted that the off-chip storage of Chong, *et al.* does not provide overflow from the cache memory. Rather, the off-chip memory statically stores all data required by the cache, and the data is retrieved for the cache as required.

With respect to claims 8-10, 23-25, 36 and 44, the Barkey and Stephens, *et al.* references do not suggest the additional level of flow control of the present invention resulting from the need to transfer information units between the first and second sets of buffers.

Although Thorson, *et al.* does suggest flits, there is no suggestion of storing those flits in a first rapidly accessible set of buffers and a second slower set of buffers.

Claim 2 has been amended for consistency with claim 1. Claim 4 has been amended to clarify the connection of the buffer array with the base claim. Claims 26 and 29 have been amended to assure proper antecedent base.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

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MARKED UP VERSION OF AMENDMENTS

Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

1. (Amended) A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers [for the] which store information units received at an input link; and

a second set of buffers for the information units that are accessed more slowly than the first set.

2. (Amended) A router as claimed in claim 1 wherein:

[the] router processing is implemented on one or more router integrated circuit chips;

the first set of buffers is located on the router integrated circuit chips; and

the second set of buffers is located on memory chips separate from the router integrated circuit chips.

4. (Amended) A router as claimed in claim 1 wherein the first set of buffers comprises:

a buffer pool; and

a pointer array of pointers to buffered information units.

16. (Amended) A method of buffering information units in a router comprising:

storing the information units received at an input link in a first set of rapidly accessible buffers; and

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set.

26. (Amended) A method as claimed in claim 16 further comprising storing information units waiting for access to the second set of [flit] buffers in miss status registers.

29. (Amended) A method as claimed in claim 16 wherein the [fabric] router is in a network switch or router.

31. (Amended) A network comprising a plurality of interconnected routers, each router including information unit buffers comprising:

a first set of rapidly accessible information unit buffers which store information units received at an input link; and

a second set of information unit buffers which store the information units and that are accessed more slowly than the first set.

40. (Amended) A router comprising:

means for storing information units received at an input link in a first set of rapidly accessible buffers; and

means for storing information units in a second set of buffers that are accessed more slowly than the first set.